L Number	Hits	Search Text	DB	Time stamp
1	1522	345/440	USPAT	2004/08/20 09:35
2	308	345/440.1	USPAT	2004/08/20 09:35
3	0	345/763345/771	USPAT	2004/08/20 09:35
4	120	717/105	USPAT	2004/08/20 09:35
5	249	717/109	USPAT	2004/08/20 09:35
6	133	717/113	USPAT	2004/08/20 09:35
7	2148	345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113	USPAT	2004/08/20 09:38
8	1839	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (connect$4 or link$4)	USPAT	2004/08/20 09:38
9	1242	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (connect$4 or link$4)same display$4	USPAT	2004/08/20 09:39
10	156	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4	USPAT	2004/08/20 10:09
11	59	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4	USPAT	2004/08/20 10:08
12	14	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (connect$4 or link$4) same (element$1 or instrument$1 or icon$1)	USPAT	2004/08/20 09:41
15	6	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (connect$4 or link$4) same (element$1 or instrument$1 or icon$1) and data near4 (transfer$4 or transmit$4 or transmiss$4 or flow$4)	USPAT	2004/08/20 09:44
16	7	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (connect$4 or link$4) same (element$1 or instrument$1 or icon$1) and (information or data) near4 (transfer$4 or transmit$4 or transmiss$4 or flow$4)	USPAT	2004/08/20 10:08
18	7	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (connect$4 or link$4) same (element$1 or instrument$1 or icon$1) and (information or data) near4 (transfer$4 or transmit$4 or transmiss$4 or flow$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:12
19	59	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:12
20	156	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:10
17	1	"20020075267" and waveform and acquisition	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:26
21	4	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4 and(waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:11
22	4	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4 and (waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:17

24	0	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (connect$4 or link$4) same (element$1 or instrument$1 or icon$1) and (information or data) near4 (transfer$4 or transmit$4 or transmiss$4 or flow$4) and (waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:12
23	2	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 and (waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:16
25	0	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and process$4 same (web or internet) same (connect$4 or link$4)same display$4 same (waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:16
26	0	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4 same (waveform near3 acquisition or waveform$1 or oscilloscope)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:16
27	4	(345/440 or 345/440.1 or 345/763345/771 or 717/105 or 717/109 or 717/113) and (web or internet) same (connect$4 or link$4)same display$4 and (waveform near3 acquisition or waveform$1 or oscilloscope) and display$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:17
28	1	"20020075267" and waveform and acquisition and process$4 near10 web	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:27
29	1	"20020075267" and waveform same acquisition and process$4 near10 web	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:27
30	1	"20020075267" and waveform same acquisition same process$4 near10 web	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/20 10:27

Brief Description
[0029] FIG. 20

Detail Descriptio
[0033] FIG. 21
constructed in ac
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automated or ma
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that are in turn c
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interface 2115.
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Detail Descriptio
[0034] Various
a preprocessing
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processing has b
display at 2150 c

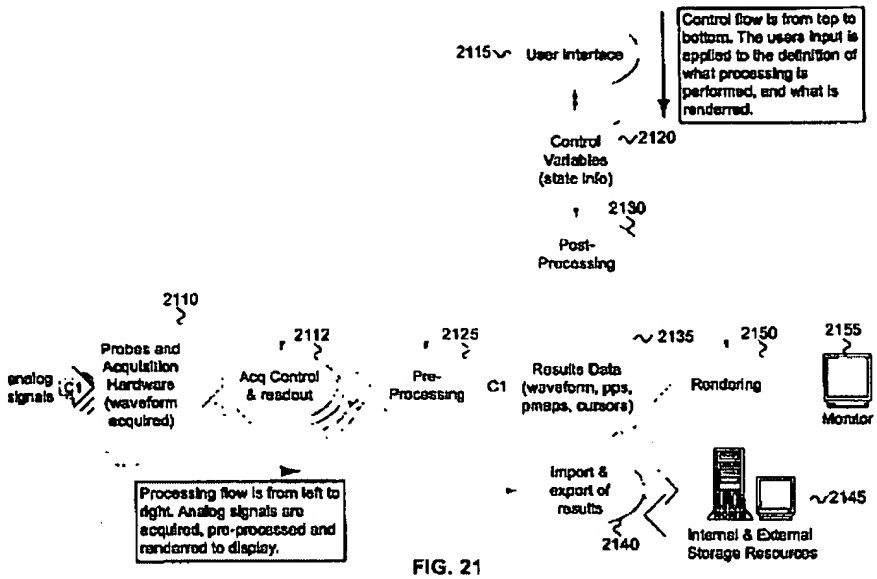


FIG. 21

resulting two-dimensional persistence map is not traditionally availa
user other than visually on the display, and therefore cannot be act
consumed by the DSO for further processing. The same applies, f
the display of two waveforms in an X vs. Y format. Thus, at this tir
flexible system for visualizing and defining an entire processing flo
DSO, from the captured waveform through to the display and/or ot
devices, in a graphical manner, does not exist.

Brief Description of Drawings Paragraph - DRTX (3):
[0010] FIG. 1 is a graphical representation of a processing web fo
LeCroy, traditional, fixed-feature instrument in accordance with the

Brief Description of Drawings Paragraph - DRTX (6):
[0013] FIG. 4 depicts a simple processing web configuration;

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):

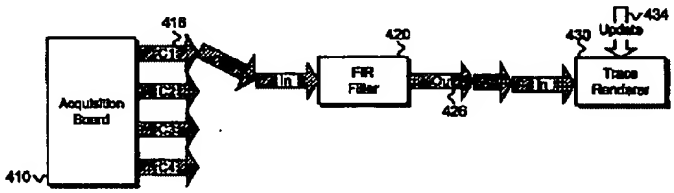


FIG. 4

resulting two-dimensional persistence map is not traditionally availa
user other than visually on the display, and therefore cannot be act
consumed by the DSO for further processing. The same applies, f
the display of two waveforms in an X vs. Y format. Thus, at this tir
flexible system for visualizing and defining an entire processing flow
DSO, from the captured waveform through to the display and/or oth
devices, in a graphical manner, does not exist.

Brief Description of Drawings Paragraph - DRTX (3):
[0010] FIG. 1 is a graphical representation of a processing web fo
LeCroy, traditional, fixed-feature instrument in accordance with the

Brief Description of Drawings Paragraph - DRTX (6):
[0013] FIG. 4 depicts a simple processing web configuration;

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web

Brief Description of Drawings Paragraph - DRTX (16):

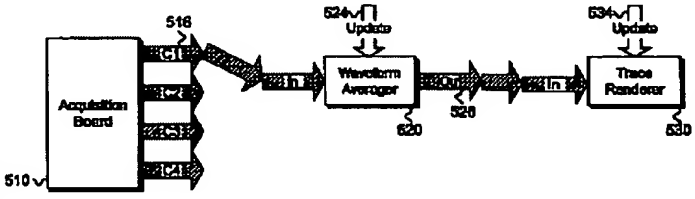


FIG. 5

resulting two-dimensional persistence map is not traditionally ava
user other than visually on the display, and therefore cannot be a
consumed by the DSO for further processing. The same applies,
the display of two waveforms in an X vs. Y format. Thus, at this t
flexible system for visualizing and defining an entire processing fl
DSO, from the captured waveform through to the display and/or c
devices, in a graphical manner, does not exist.

Brief Description of Drawings Paragraph - DRTX (3):
[0010] FIG. 1 is a graphical representation of a processing web
LeCroy, traditional, fixed-feature instrument in accordance with th

Brief Description of Drawings Paragraph - DRTX (6):
[0013] FIG. 4 depicts a simple processing web configuration;

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):

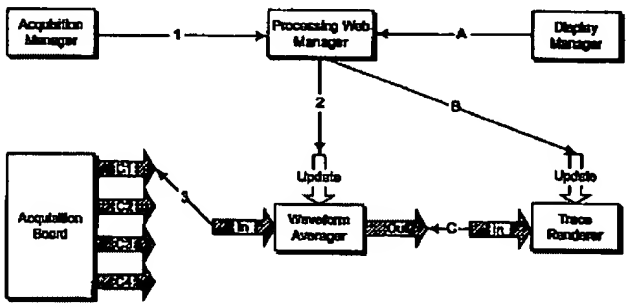


FIG. 6

resulting two-dimensional persistence map is not traditionally ava
user other than visually on the display, and therefore cannot be a
consumed by the DSO for further processing. The same applies,
the display of two waveforms in an X vs. Y format. Thus, at this t
flexible system for visualizing and defining an entire processing fl
DSO, from the captured waveform through to the display and/or c
devices, in a graphical manner, does not exist.

Brief Description of Drawings Paragraph - DRTX (3):
[0010] FIG. 1 is a graphical representation of a processing web
LeCroy, traditional, fixed-feature instrument in accordance with th

Brief Description of Drawings Paragraph - DRTX (6):
[0013] FIG. 4 depicts a simple processing web configuration;

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):

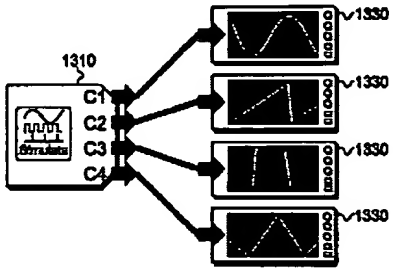


FIG. 13

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processin

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):
[0023] FIG. 14 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (17):
[0024] FIG. 15 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (18):
[0025] FIG. 16 is a flowchart depicting a sequence for populatin processing web editor screen in accordance with an existing proc

Brief Description of Drawings Paragraph - DRTX (19):
[0026] FIG. 17 is a flowchart depicting a sequence for dropping component into a processing web using a processing web editor;

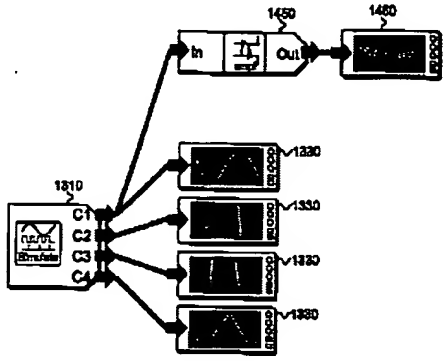


FIG. 14

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):
[0023] FIG. 14 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (17):
[0024] FIG. 15 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (18):
[0025] FIG. 16 is a flowchart depicting a sequence for populatin processing web editor screen in accordance with an existing proc

Brief Description of Drawings Paragraph - DRTX (19):
[0026] FIG. 17 is a flowchart depicting a sequence for dropping component into a processing web using a processing web editor;

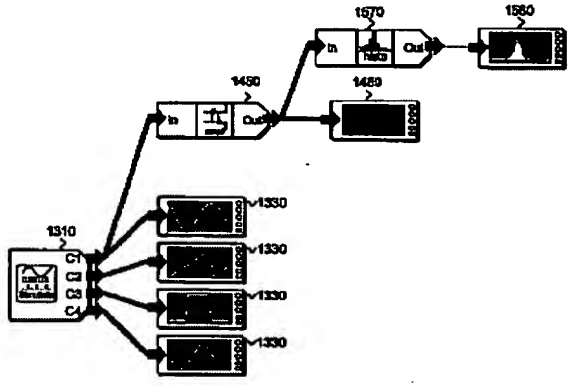


FIG. 15

Brief Description of Drawings Paragraph - DRTX (7):
[0014] FIG. 5 depicts a further processing web configuration;

Brief Description of Drawings Paragraph - DRTX (8):
[0015] FIG. 6 depicts separate processing paths in a processing

Brief Description of Drawings Paragraph - DRTX (15):
[0022] FIG. 13 depicts a simple form of a processing web;

Brief Description of Drawings Paragraph - DRTX (16):
[0023] FIG. 14 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (17):
[0024] FIG. 15 depicts a further form of a processing web;

Brief Description of Drawings Paragraph - DRTX (18):
[0025] FIG. 16 is a flowchart depicting a sequence for populatin processing web editor screen in accordance with an existing proc

Brief Description of Drawings Paragraph - DRTX (19):
[0026] FIG. 17 is a flowchart depicting a sequence for dropping component into a processing web using a processing web editor;

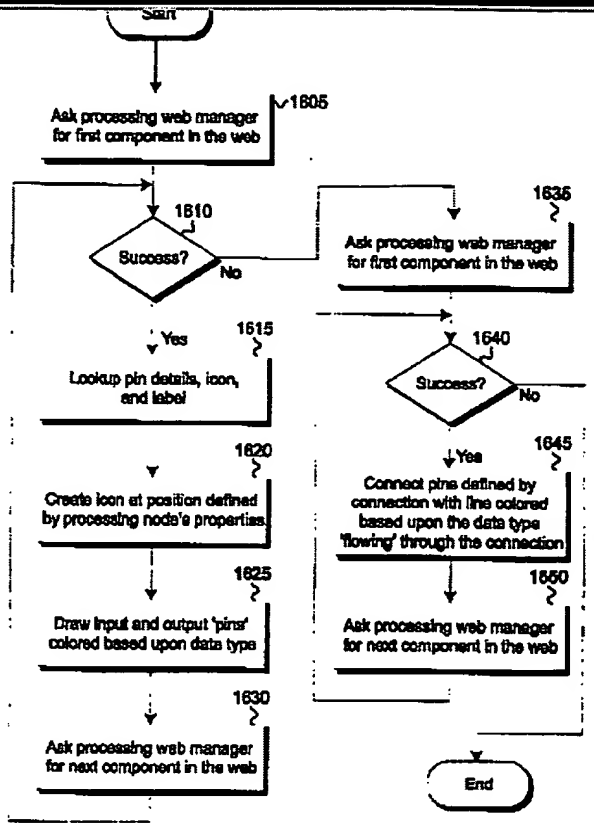


FIG. 16

Brief Description of Drawings Paragraph - DRTX (18):
[0025] FIG. 16 is a flowchart depicting a sequence for populatin processing web editor screen in accordance with an existing proc

Brief Description of Drawings Paragraph - DRTX (19):
[0026] FIG. 17 is a flowchart depicting a sequence for dropping component into a processing web using a processing web editor;

Brief Description of Drawings Paragraph - DRTX (20):
[0027] FIG. 18 is a flowchart depicting a sequence for attemptin two pins in a processing web using a processing web editor;

Brief Description of Drawings Paragraph - DRTX (21):
[0028] FIG. 19 is a view of a functioning processing web editor;

Brief Description of Drawings Paragraph - DRTX (22):
[0029] FIG. 20 is a further view of a functioning processing web

Detail Description Paragraph - DETX (4):
[0033] FIG. 21 depicts a conceptualized notion of how the oscill constructed in accordance with the invention operates. The flow shown from left to right and control sequences provided by a user automated or manual, are shown from top down. As is shown in plurality of analog acquisition signals C.sub.1 are acquired by the oscilloscope of the invention. These acquisition signals are acqu accordance with various provided probes and other acquisition ha

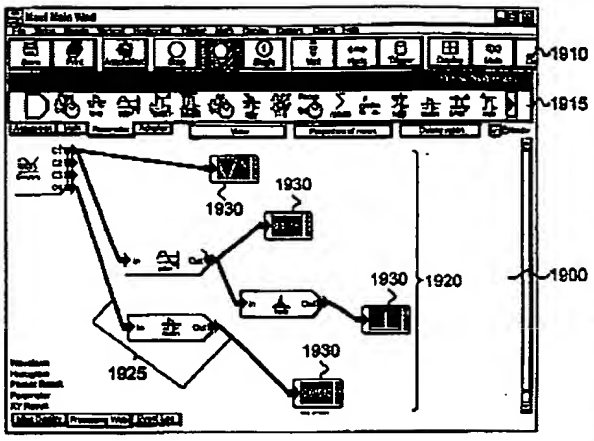


FIG. 19

Brief Description of Drawings Paragraph - DRTX (18):
[0025] FIG. 16 is a flowchart depicting a sequence for populatin processing web editor screen in accordance with an existing proc

Brief Description of Drawings Paragraph - DRTX (19):
[0026] FIG. 17 is a flowchart depicting a sequence for dropping component into a processing web using a processing web editor;

Brief Description of Drawings Paragraph - DRTX (20):
[0027] FIG. 18 is a flowchart depicting a sequence for attemptin two pins in a processing web using a processing web editor;

Brief Description of Drawings Paragraph - DRTX (21):
[0028] FIG. 19 is a view of a functioning processing web editor;

Brief Description of Drawings Paragraph - DRTX (22):
[0029] FIG. 20 is a further view of a functioning processing web

Detail Description Paragraph - DETX (4):
[0033] FIG. 21 depicts a conceptualized notion of how the oscill constructed in accordance with the invention operates. The flow shown from left to right and control sequences provided by a user automated or manual, are shown from top down. As is shown in plurality of analog acquisition signals C.sub.1 are acquired by the oscilloscope of the invention. These acquisition signals are acqui accordance with various provided probes and other acquisition ha

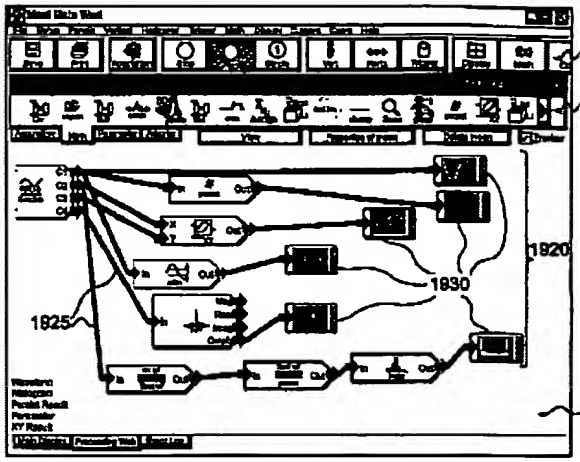


FIG. 20

US-PAT-NO: 67005

DOCUMENT-IDENTIFIER:

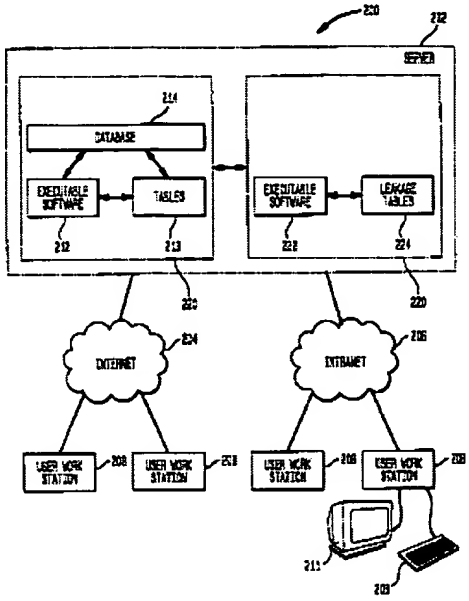
TITLE: Methods a management

-------- KWIC --------

Detailed Description Text - Because of the implicatio presently a PCMS program system, thought should be g are defined. Analysts shou to implement this feature. T charts. The "auto add" feat charts. Rather than manua may be entered in the datat type of chart to be created i When data begins to flow in the chart name is compared automatically create a chart notifying the user of the cha

Detailed Description Text - If "L Charts" was selected exemplary L charts page 12

FIG. 2



US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic information flow method and system analyzing patterns and relationships

-------- KWIC --------

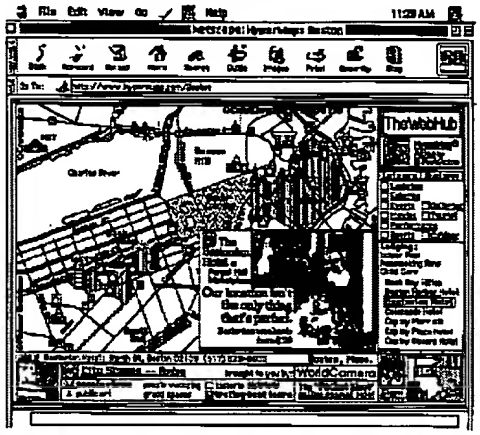
Abstract Text - ABTX (1):
A novel display control and information management system integrates layered and slotted formatted data from both local a sources to provide a highly versatile information display. The s selective control of display so that complex data and data flows seamlessly accessed with enhanced cognition of salient inform

TITLE - TI (1):
Graphic information flow method and system for visually ana and relationships

Brief Summary Text - BSTX (9):
A typical GIS often also has a large database with thematic i places on the map. However, current GIS does not provide fo to subset combinations from extensive data sets. A legend, ta or key shows a small selection of themes and the symbols ass subsets within each theme. In some cases, entire themes may by clicking a check box next to the theme title on the legend h

Details Text Image HTML KWIC

FIG. 6d Alternative Presentations



Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic-information flow method and system analyzing patterns and relationships

-------- KWIC --------

Abstract Text - ABTX (1):
A novel display control and information management system integrates layered and slotted formatted data from both local a sources to provide a highly versatile information display. The s selective control of display so that complex data and data flows seamlessly accessed with enhanced cognition of salient inform

TITLE - TI (1):
Graphic-information flow method and system for visually ana and relationships

Brief Summary Text - BSTX (9):
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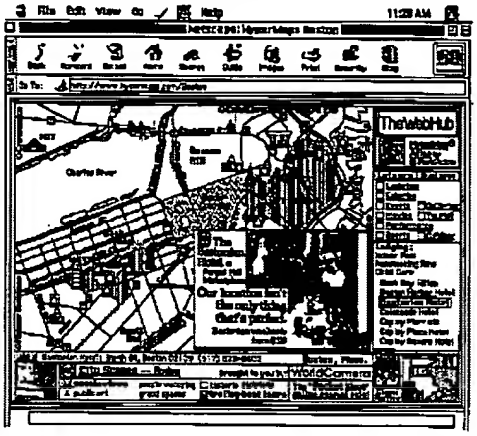
Details Text Image HTML KWIC

FIG. 6d Alternative Presentations



Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic-information flow method and system analyzing patterns and relationships

-------- KWIC --------

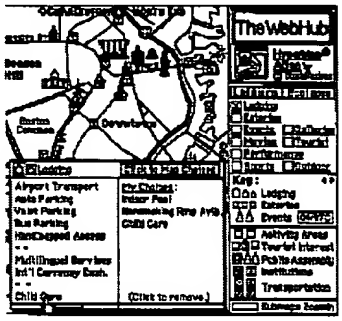
Abstract Text - ABTX (1):
A novel display control and information management system integrates layered and slotted formatted data from both local a sources to provide a highly versatile information display. The s selective control of display so that complex data and data flows seamlessly accessed with enhanced cognition of salient inform

TITLE - TI (1):
Graphic-information flow method and system for visually ana and relationships

Brief Summary Text - BSTX (9):
A typical GIS often also has a large database with thematic i places on the map. However, current GIS does not provide fo to subset combinations from extensive data sets. A legend, ta or key shows a small selection of themes and the symbols ass subsets within each theme. In some cases, entire themes may by clicking a check box next to the theme title on the legend, h

Details Text Image HTML KWIC

FIG. 6e Alternative Presentations



Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic information flow method and system analyzing patterns and relationships

-------- KWIC -------

Abstract Text - ABTX (1):

A novel display control and information management system integrates layered and slotted formatted data from both local a sources to provide a highly versatile information display. The s selective control of display so that complex data and data flows seamlessly accessed with enhanced cognition of salient inform

TITLE - TI (1):

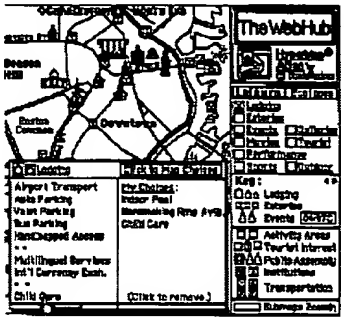
Graphic information flow method and system for visually ana and relationships

Brief Summary Text - BSTX (9):

A typical GIS often also has a large database with thematic i places on the map. However, current GIS does not provide fo to subset combinations from extensive data sets. A legend, ta or key shows a small selection of themes and the symbols ass subsets within each theme. In some cases, entire themes ma by clicking a checkbox next to the theme title on the legend h

Details Text Image HTML KWIC

FIG. 6e Alternative Presentations



Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic-information flow method and system analyzing patterns and relationships

-------- KWIC -------

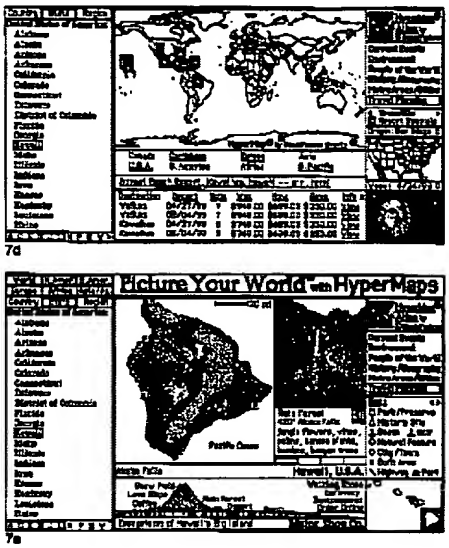
Abstract Text - ABTX (1):
A novel display control and information management system integrates layered and slotted formatted data from both local a sources to provide a highly versatile information display. The selective control of display so that complex data and data flows seamlessly accessed with enhanced cognition of salient inform

TITLE - TI (1):
Graphic-information flow method and system for visually an and relationships

Brief Summary Text - BSTX (9):
A typical GIS often also has a large database with thematic i places on the map. However, current GIS does not provide fo to subset combinations from extensive data sets. A legend, ta or key shows a small selection of themes and the symbols ass subsets within each theme. In some cases, entire themes ma by clicking a check box next to the theme title on the legend h

Details Text Image HTML KWIC

FIG. 7de A Seamless Stream of Display Screens



Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic-information flow method and system analyzing patterns and relationships

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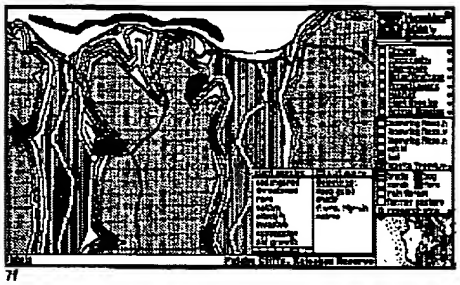
Details Text Image HTML KWIC

FIG. 7fg A Seamless Stream of Display Screens



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Details Text Image HTML Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic information flow method and system analyzing patterns and relationships

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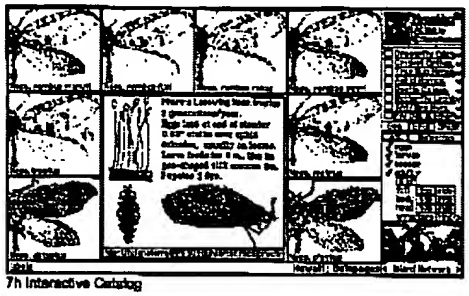
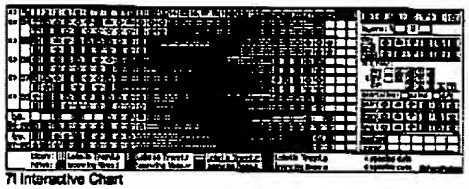
Details | Text | Image | HTML | KWIC

FIG. 7hl A Seamless Stream of Display Screens



7h Interactive Catalog



7i Interactive Chart

Details | Text | Image | HTML | Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic-information flow method and system analyzing patterns and relationships

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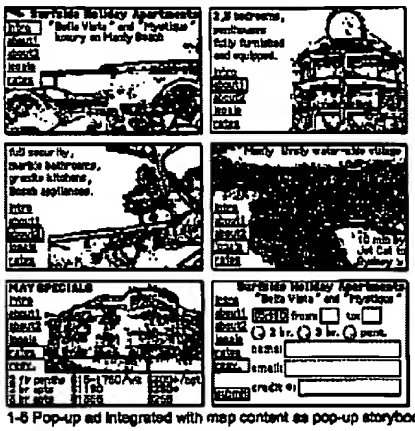
Details | Text | Image | HTML | KWIC

FIG. 9a-B Integrated Informational Advertising



1-5 Pop-up ad integrated with map content as pop-up storybook.

Details | Text | Image | HTML | Full

US-PAT-NO: 6307573

DOCUMENT-IDENTIFIER: US 6307573 B1

TITLE: Graphic information flow method and system analyzing patterns and relationships

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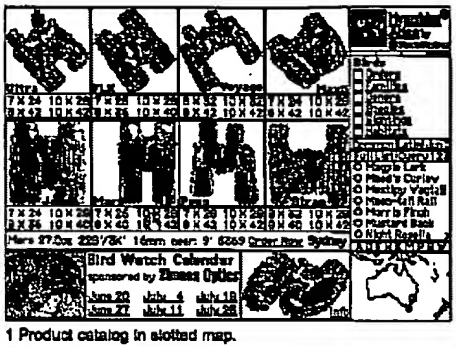
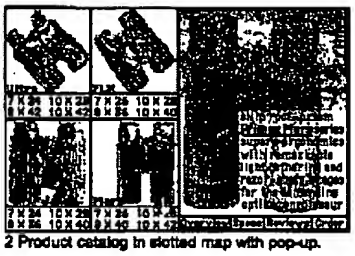
Details Text Image HTML KWIC

FIG. 9c Integrated Informational Advertising



1 Product catalog in slotted map.



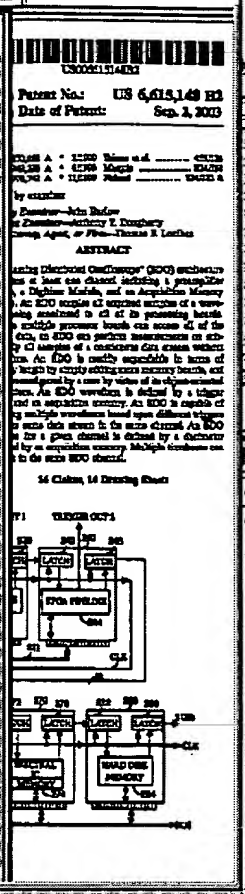
2 Product catalog in slotted map with pop-up.

Details Text Image HTML Full

Detailed Description Text - DETX (13):
A D/A converter board 250 can be inserted between any of the processor boards in the chain to generate analog output signals as needed. A typical D/A Converter board includes an input FIFO 252, a D/A Converter circuit 254, and an output FIFO 256 for coupling the data stream to the next board in sequence. D/A converter board 250 can be used to trigger an external oscilloscope or other test equipment (not shown). D/A converter board 250 may also be used to provide external control signals or signals for external monitoring of continuous measurement results. A MEMORY BOARD 260, 270 can be located at any place in the data stream, and can be used, for example, to create a DPO data base or capture frames of data for display.

Detailed Description Text - DETX (14):
An ACQUISITION MEMORY BOARD 260 is configured to receive an input data stream and to output the data stream to the next board in the pipeline. Upon receipt of a trigger line signal from one of the previous FPGA boards 230, 240, a frame of data would be captured and stored. This frame is then made available to the PC bus 201 where it will be applied to a display (not shown). Memory boards (or modules) have multiple trigger inputs so that it is possible to capture waveforms based upon different kinds of triggers in different parts of the data stream.

Detailed Description Text - DETX (16):
Other kinds of boards such as, signal generators, spectrum analyzers, and other processing modules may be inserted anywhere in the data stream, as needed.



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EAST Browser - L58: (1) (702/66 or 7... | US 6615148 B2 | Tag: S,T1 | Doc: 1/1 | Format : KWIC

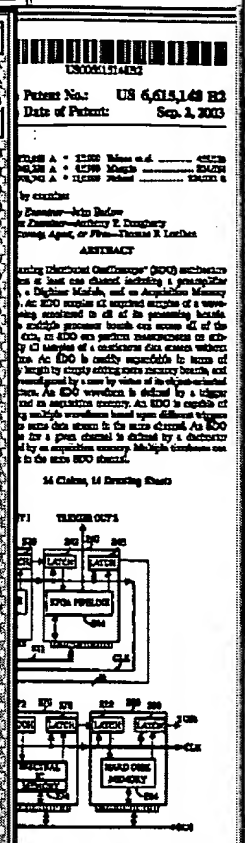
File Edit View Tools Window Help

Detailed Description Text - DETX (3):
Referring to FIG. 1, an architecture for a typical digital storage oscilloscope 100, as known from the prior art, comprises a serial arrangement of a Preamplifier 110, an A/D Converter 120, a Demultiplexer (Demux) 130, an Acquisition Memory 140, a controller (microprocessor, or .P) 150, a Display Memory 160, and a Display unit 170, in that order. This kind of arrangement is typically configured on one or two printed circuit boards and is not reconfigurable by a user.

Detailed Description Text - DETX (6):
The SDO architecture is designed so that each kind of module in the data stream has a standard set of attributes. With this approach a new preamplifier can be designed and plugged into the system without changing any of the SW on the PC side of the interface. A new memory board can be designed and installed with no changes except to the memory board itself.

Detailed Description Text - DETX (7):
It is important to note that by use of the streaming distributed oscilloscope architecture, a new custom application comprising both hardware and software components can be developed in 3 to 6 months. Even more significant is the fact that with standard available streaming scope module options and their libraries, new application configurations can be developed in a matter of minutes, rather than weeks.

Detailed Description Text - DETX (8):
In this regard, note that any number of channels is possible because of the



EAST - [09861469new.wsp:1]

EAST Browser - L57: (6) (702/66 or 7... | US 6615148 B2 | Tag: S,T1 | Doc: 2/6 | Format : KWIC

File Edit View Tools Window Help

Detailed Description Text - DETX (67):

A Processor Module is capable of performing measurements on, or applying signal processing algorithms to, the stream of data as it passes from the input to the output of the module. The measurements that it performs may be compared against levels and used as triggers. A processor board may have multiple trigger outputs, and it is herein recognized that Processor Modules may have trigger input signals. These trigger input signals can be used by the Processor Module in various ways that will depend on the library of functions that are created for a particular processor. For example, trigger input signals may act as triggers to arm the Processor Module to make measurements. Some processor boards may be configured using FPGAs and some may use standard DSP chips. However, each will have its own library of trigger sources. The purpose of the Trigger source window menu is to allow the user to select the trigger type that is assigned to the trigger outputs of processor boards.

Detailed Description Text - DETX (68):

FIG. 15 is a simplified circuit block diagram of the Stream Splitter 1010 of Acquisition Memory Module 1000 of FIG. 10. In its simplest form, Stream Splitter 1010 comprises a clocked input latch 1505 for receiving at least one data stream, a buffer array 1515 for providing lathed data to Demultiplexer circuit 1020, a clocked output latch 1510, and an output buffer array 1520 for passing the data stream or streams to the next module in the sequence.

Detailed Description Text - DETX (69):

The following is a list of parameters that the system controller PC may set and/or read for a memory board. The parameters have been chosen so that the different board models may have different numbers of input streams or triggers

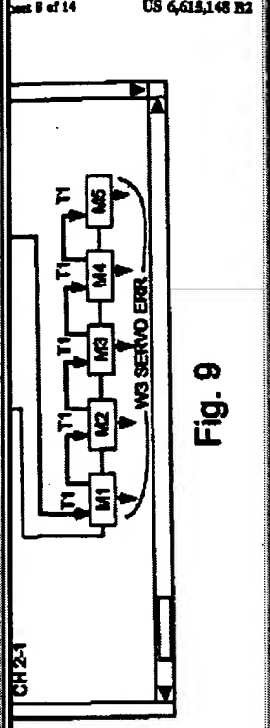


Fig. 9

parts of an SDO system from one central location via the Internet.

Detailed Description Text - DETX (32):

FIG. 8 is a screen display showing defined waveforms for an SDO system. Each waveform in an SDO system is defined by a particular active trigger applied to a particular Acquisition Memory Module. The term "active" means that a trigger source has been connected to a trigger input and that the waveform has been defined as shown in the window display of FIG. 8. The "Define Waveforms, Trigger Receivers" menu allows the user to define waveforms by assigning processor trigger sources to Acquisition Memory Module input trigger terminals. This menu allows the user to define the receivers of triggers and assign a waveform ID and name label to a particular waveform. A "Define Trigger Sources" menu (not shown) allows the user to define the sources of triggers, and to define what kind of event will cause each trigger. Trigger sources are either external, or from a processor module or from another memory module.

Detailed Description Text - DETX (34):

Referring to FIG. 9, the hardward blocks located in a given channel are sensed by the system controller PC and a schematic is automatically drawn in a screen display. A configuration of this hardware may be altered by dragging and dropping various blocks in the window display of FIG. 9, and connecting the blocks as desired. The user completes trigger connections by means of a mouse or other drawing capabilities. Operating graphically on the schematic of FIG. 9 will affect the waveform list of FIG. 8, which will change to match the new configuration. Conversely, altering the list of FIG. 8 will cause a change in the schematic channel representation of FIG. 9.

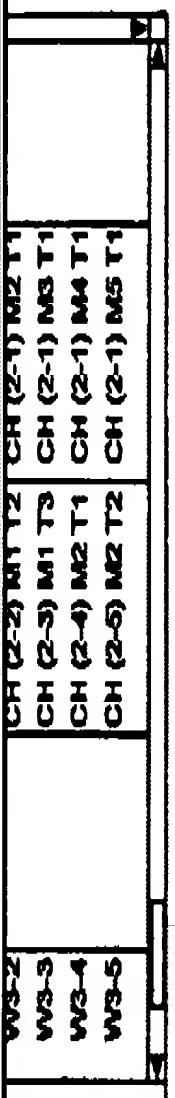


Fig. 8

data and how quickly a user can obtain a processing result. Moreover, the total complexity of the processing is limited by the host computer's resource limits.

Detailed Description Text - DETX (26):

The functionality of the present invention's streaming architecture, as described herein, is applicable to the processing web described in Provisional U.S. Patent Application No. 60/249,482, filed Nov. 17, 2000, the entire contents thereof being incorporated herein by reference. The processing web provides an oscilloscope design that is completely "modular," whereby the elements comprising the oscilloscope are completely specified in terms of interface, and are sufficiently independent in construction that they can be installed and removed at run-time (e.g. without stopping the process which can be considered the oscilloscope application software). Basically, there is no limit to the permitted complexity of a given "processing web."

Detailed Description Text - DETX (27):

The processing web supports the use of multiple processing objects which may be chained together, utilizing multiple inputs and producing multiple outputs. Processors may be used to produce data for more than one further processor. Each processing object receives certain inputs (according to various input requirements) and generates particular output types (e.g. parameters, persistence maps or waveforms). These processing objects also have particular update or synchronization characteristics for obtaining or generating information, and can be expressed using a same generic processor model, but being designated according to a variable number and type of input, output and update pins.

Detailed Description Text - DETX (37):

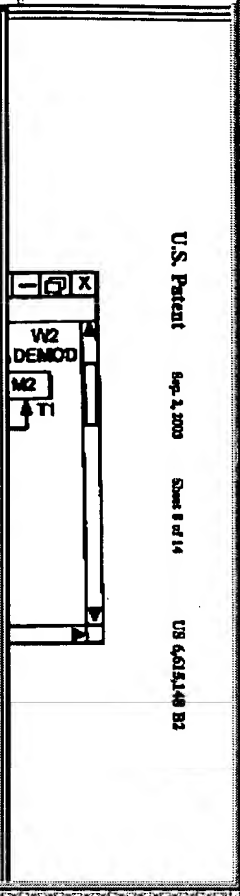
It is important to note that every waveform in the system must have a trigger. Even if there were only one acquisition memory module in the channel, it is possible to have up to 32 waveforms defined that can be triggered and captured within that memory. For that case, all waveforms acquired would have a different time stamp. For the case where all channels are to be acquired with the same time stamp it would be necessary to have a separate Acquisition Memory Module for each waveform. Typical SDO Acquisition Memory Module memories will contain one, two, or four input data streams, and can store 1, 2, or 4 waveforms simultaneously. At least one trigger connection is needed for each memory board that is contained in the system.

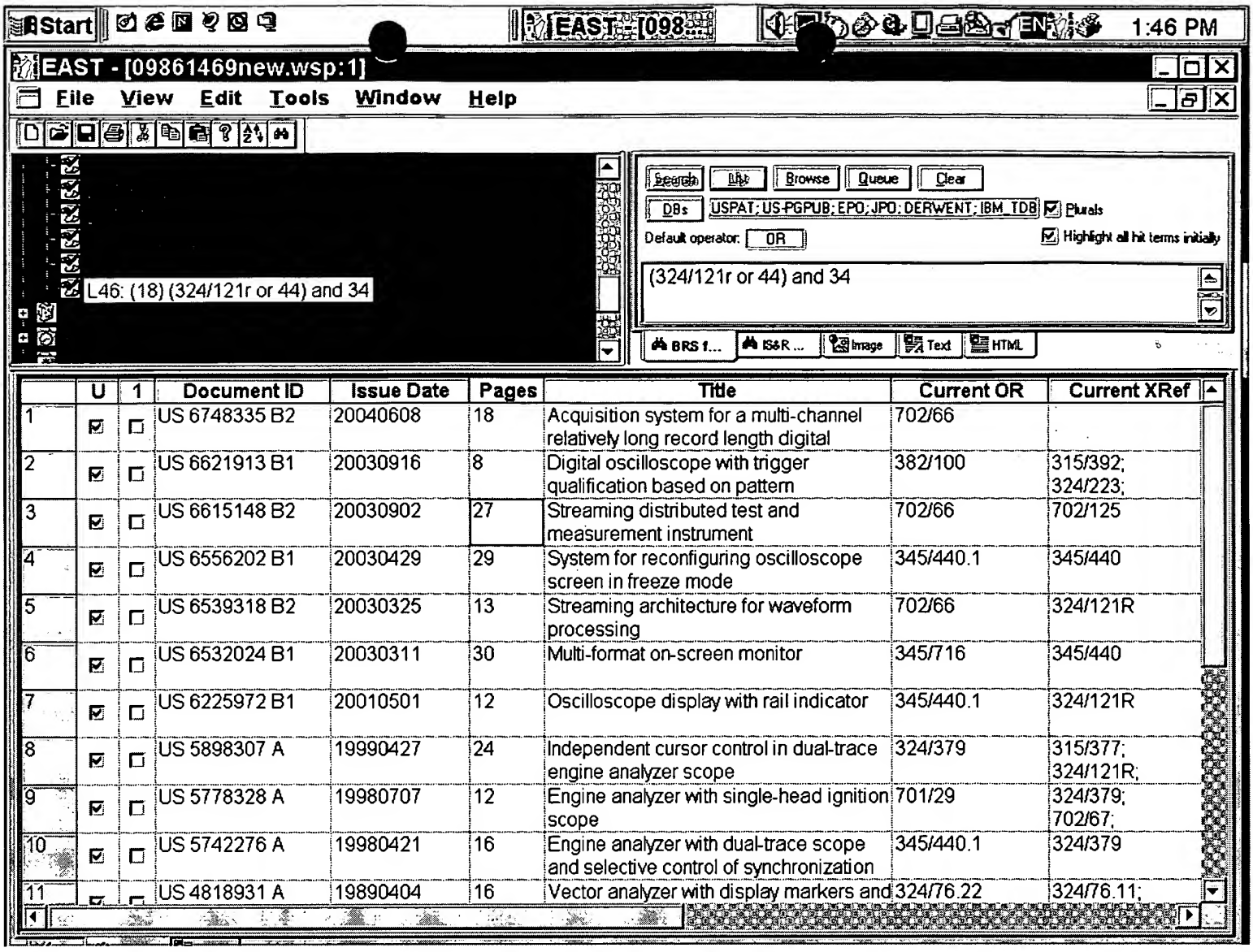
Detailed Description Text - DETX (42):

As shown in the screen display of FIG. 9, system software can detect the modules plugged into the bus and display a block diagram of the current system configuration. Selecting a block in the processing block diagram would bring up the configuration menu that allows the customer to set the control parameters for that particular board. If the selected block is a processor board then available measurements or signal processing functions may be selected. With this approach, system hardware modules can be configured in any order or different kinds of boards may be employed, as desired. No new software design or hardware design is needed in order to configure the new system. A default setup can be used and the customer can change it to obtain any kind of process or measurement available in the system software libraries.

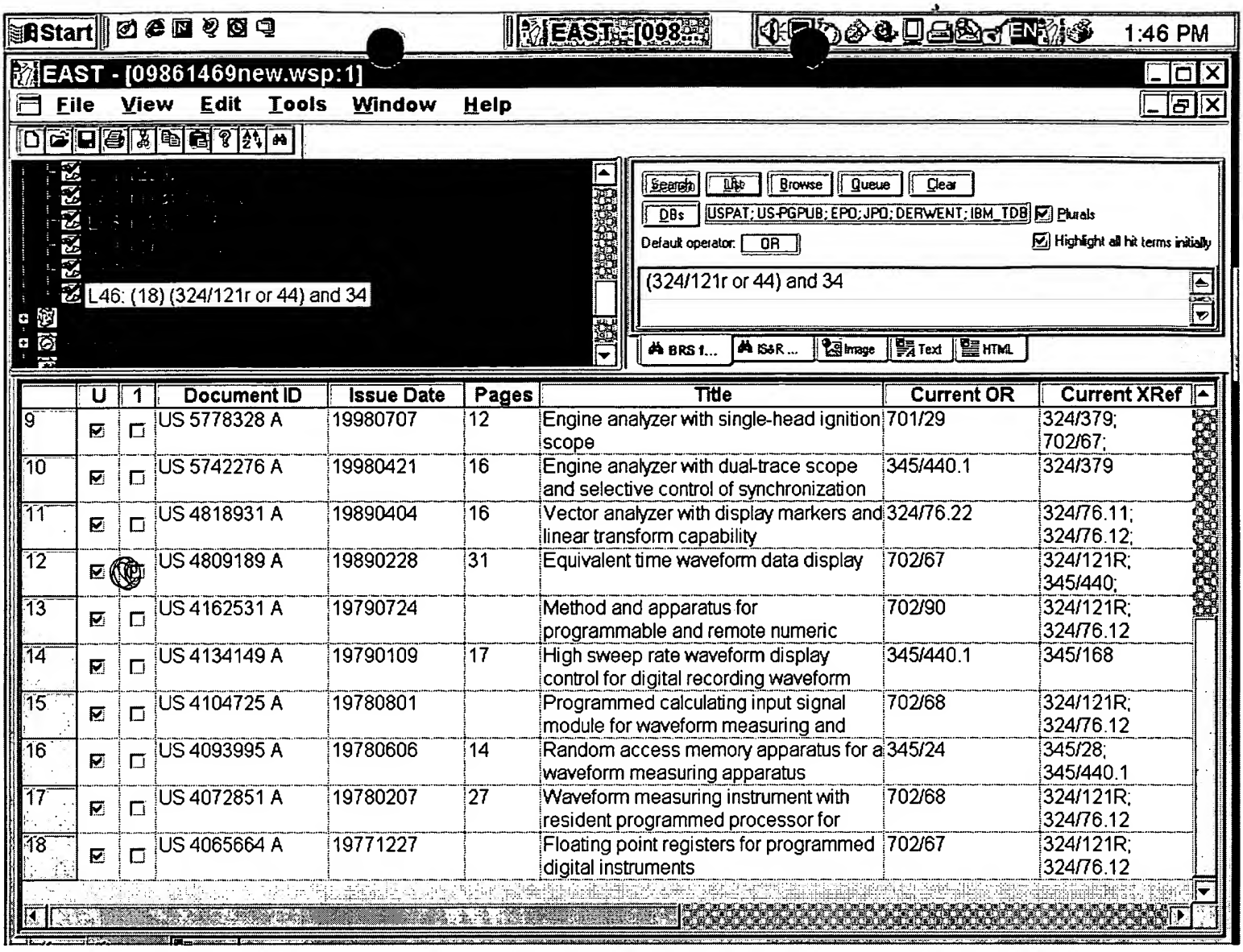
Detailed Description Text - DETX (43):

FIG. 10 is a more detailed illustration of ACQUISITION MEMORY BOARD 260 of FIG. 2. A Stream Splitter unit 1010 of Acquisition Memory Module 1000 receives

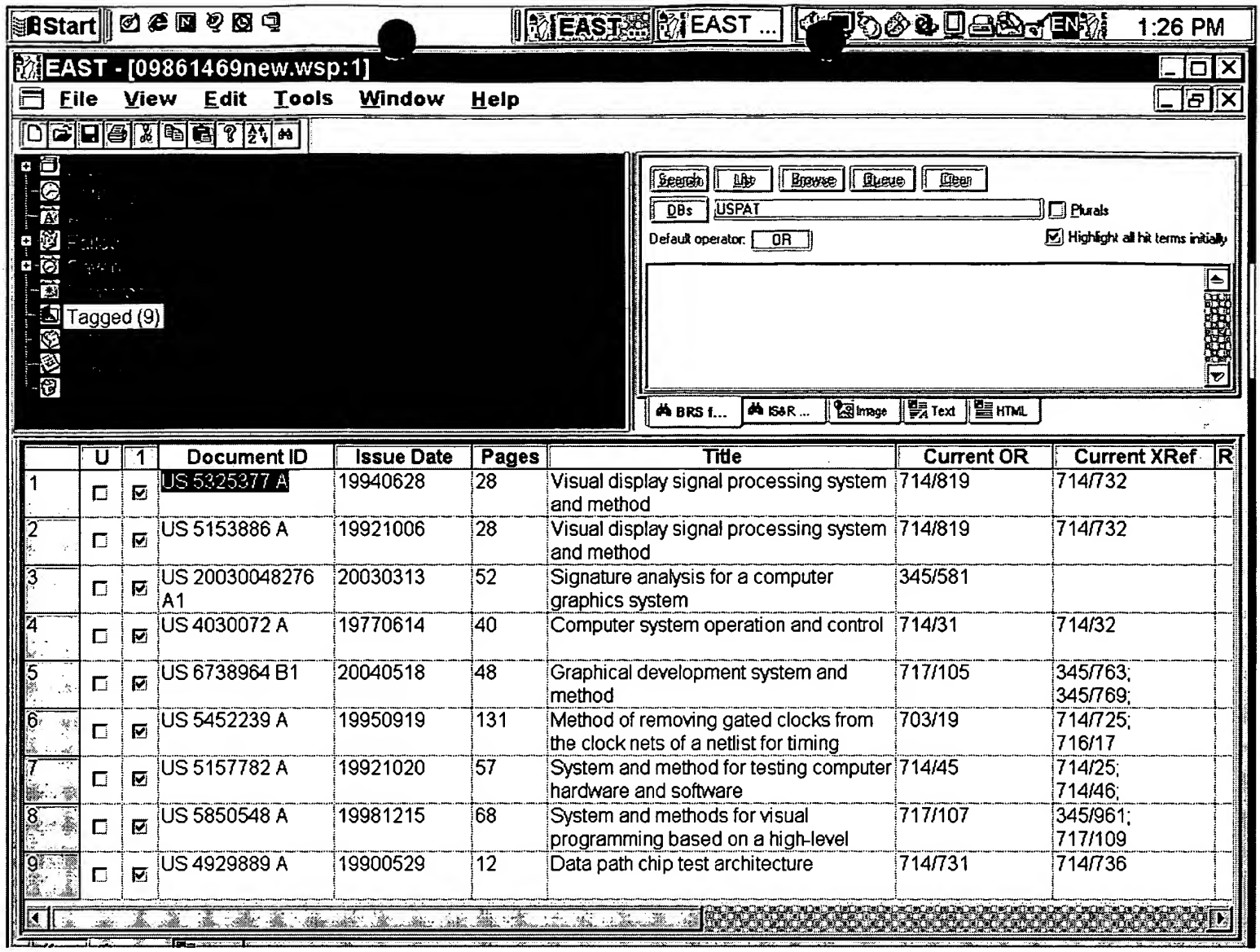




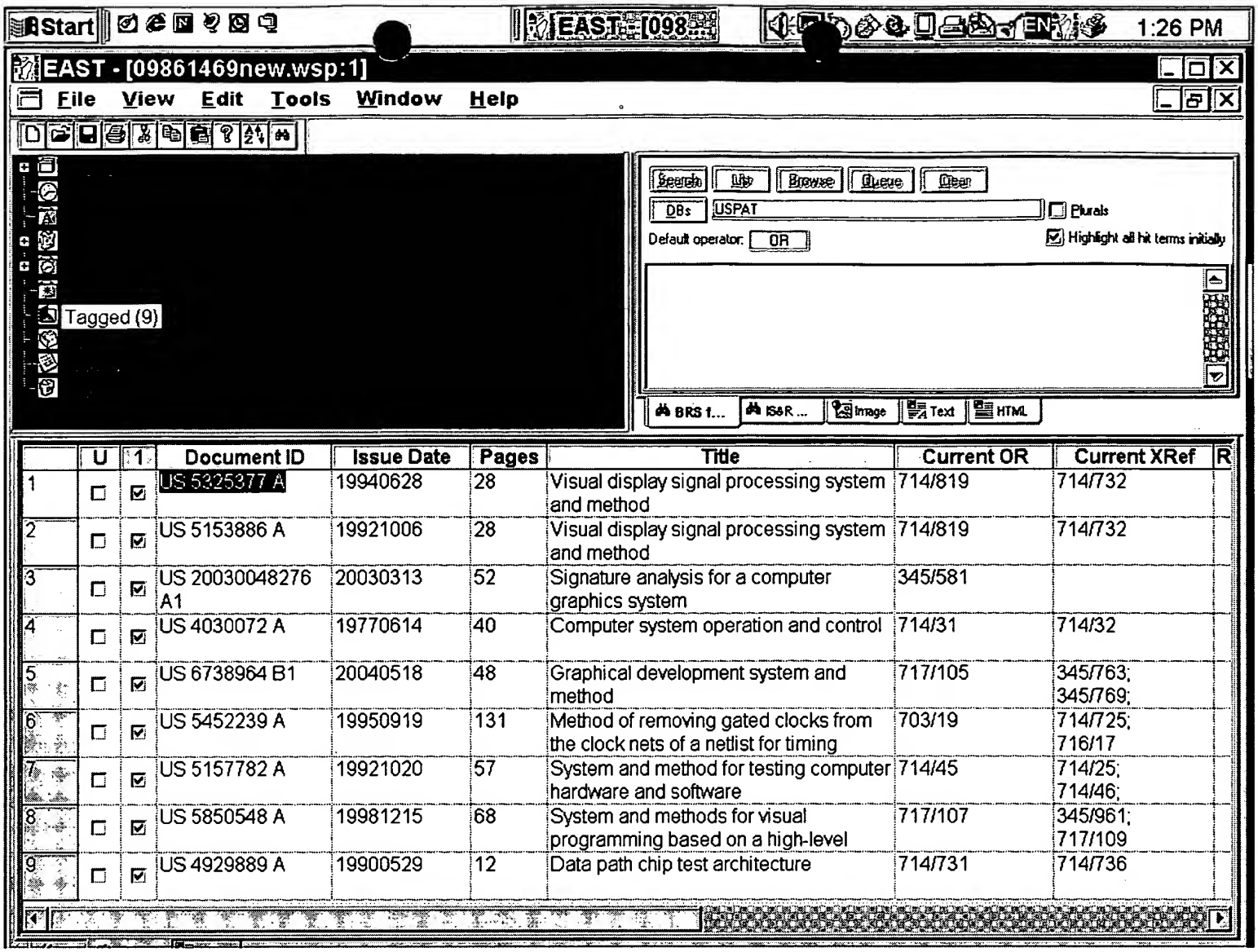
	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☑	☐	US 6748335 B2	20040608	18	Acquisition system for a multi-channel relatively long record length digital	702/66	
2	☑	☐	US 6621913 B1	20030916	8	Digital oscilloscope with trigger qualification based on pattern	382/100	315/392; 324/223;
3	☑	☐	US 6615148 B2	20030902	27	Streaming distributed test and measurement instrument	702/66	702/125
4	☑	☐	US 6556202 B1	20030429	29	System for reconfiguring oscilloscope screen in freeze mode	345/440.1	345/440
5	☑	☐	US 6539318 B2	20030325	13	Streaming architecture for waveform processing	702/66	324/121R
6	☑	☐	US 6532024 B1	20030311	30	Multi-format on-screen monitor	345/716	345/440
7	☑	☐	US 6225972 B1	20010501	12	Oscilloscope display with rail indicator	345/440.1	324/121R
8	☑	☐	US 5898307 A	19990427	24	Independent cursor control in dual-trace engine analyzer scope	324/379	315/377; 324/121R;
9	☑	☐	US 5778328 A	19980707	12	Engine analyzer with single-head ignition scope	701/29	324/379; 702/67;
10	☑	☐	US 5742276 A	19980421	16	Engine analyzer with dual-trace scope and selective control of synchronization	345/440.1	324/379
11	☑	☐	US 4818931 A	19890404	16	Vector analyzer with display markers and	324/76.22	324/76.11;



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
9	☑	☐	US 5778328 A	19980707	12	Engine analyzer with single-head ignition scope	701/29	324/379; 702/67;
10	☑	☐	US 5742276 A	19980421	16	Engine analyzer with dual-trace scope and selective control of synchronization	345/440.1	324/379
11	☑	☐	US 4818931 A	19890404	16	Vector analyzer with display markers and linear transform capability	324/76.22	324/76.11; 324/76.12;
12	☑	☐	US 4809189 A	19890228	31	Equivalent time waveform data display	702/67	324/121R; 345/440;
13	☑	☐	US 4162531 A	19790724		Method and apparatus for programmable and remote numeric	702/90	324/121R; 324/76.12
14	☑	☐	US 4134149 A	19790109	17	High sweep rate waveform display control for digital recording waveform	345/440.1	345/168
15	☑	☐	US 4104725 A	19780801		Programmed calculating input signal module for waveform measuring and	702/68	324/121R; 324/76.12
16	☑	☐	US 4093995 A	19780606	14	Random access memory apparatus for a waveform measuring apparatus	345/24	345/28; 345/440.1
17	☑	☐	US 4072851 A	19780207	27	Waveform measuring instrument with resident programmed processor for	702/68	324/121R; 324/76.12
18	☑	☐	US 4065664 A	19771227		Floating point registers for programmed digital instruments	702/67	324/121R; 324/76.12



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☑	US 5325377 A	19940628	28	Visual display signal processing system and method	714/819	714/732	
2	☐	☑	US 5153886 A	19921006	28	Visual display signal processing system and method	714/819	714/732	
3	☐	☑	US 20030048276 A1	20030313	52	Signature analysis for a computer graphics system	345/581		
4	☐	☑	US 4030072 A	19770614	40	Computer system operation and control	714/31	714/32	
5	☐	☑	US 6738964 B1	20040518	48	Graphical development system and method	717/105	345/763; 345/769;	
6	☐	☑	US 5452239 A	19950919	131	Method of removing gated clocks from the clock nets of a netlist for timing	703/19	714/725; 716/17	
7	☐	☑	US 5157782 A	19921020	57	System and method for testing computer hardware and software	714/45	714/25; 714/46;	
8	☐	☑	US 5850548 A	19981215	68	System and methods for visual programming based on a high-level	717/107	345/961; 717/109	
9	☐	☑	US 4929889 A	19900529	12	Data path chip test architecture	714/731	714/736	



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☑	US 5325377 A	19940628	28	Visual display signal processing system and method	714/819	714/732	
2	☐	☑	US 5153886 A	19921006	28	Visual display signal processing system and method	714/819	714/732	
3	☐	☑	US 20030048276 A1	20030313	52	Signature analysis for a computer graphics system	345/581		
4	☐	☑	US 4030072 A	19770614	40	Computer system operation and control	714/31	714/32	
5	☐	☑	US 6738964 B1	20040518	48	Graphical development system and method	717/105	345/763; 345/769;	
6	☐	☑	US 5452239 A	19950919	131	Method of removing gated clocks from the clock nets of a netlist for timing	703/19	714/725; 716/17	
7	☐	☑	US 5157782 A	19921020	57	System and method for testing computer hardware and software	714/45	714/25; 714/46;	
8	☐	☑	US 5850548 A	19981215	68	System and methods for visual programming based on a high-level	717/107	345/961; 717/109	
9	☐	☑	US 4929889 A	19900529	12	Data path chip test architecture	714/731	714/736	

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TITLE: Digital signa
displaying trans
transmission sy

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Summary of Invention Paragra

[0082] According to still anot
a method of displaying a digita
signal receiver. A digital signa
digital signal transmitter using
comprises the steps of proces
processing unit of the digital si
demodulated signal and a corr
signal processing unit, generat
condition including a main way
a signal converter coupled with
displaying the waveform indica
signal on a display.

Detail Description Paragraph

[0252] Thus, in this embodir
ghost status is displayed in the
with the display resolution or c
provided in the lateral direction

US 20010024468A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2001/0024468 A1

Miyashita et al. (43) Pub. Date: Sep. 27, 2001

(54) DIGITAL SIGNAL TRANSMISSION SYSTEM AND METHOD OF DISPLAYING TRANSMISSION CONDITION IN DIGITAL SIGNAL TRANSMISSION SYSTEM

(76) Inventors: Atsushi Miyashita, Tokorozawa (JP); Toshikazu Wagatsuma, Kodaira (JP); Hiroyuki Tanaka, Kodaira (JP)

Correspondence Address:
ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

(21) Appl. No.: 09/861,469

(22) Filed: May 22, 2001

(30) Foreign Application Priority Data

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Aug. 24, 2000 (JP) 2000-253618
Sep. 12, 2000 (JP) 2000-276772

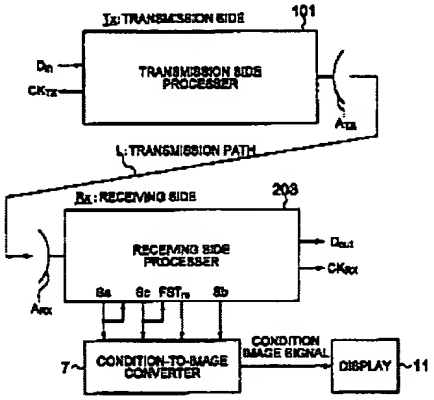
Publication Classification

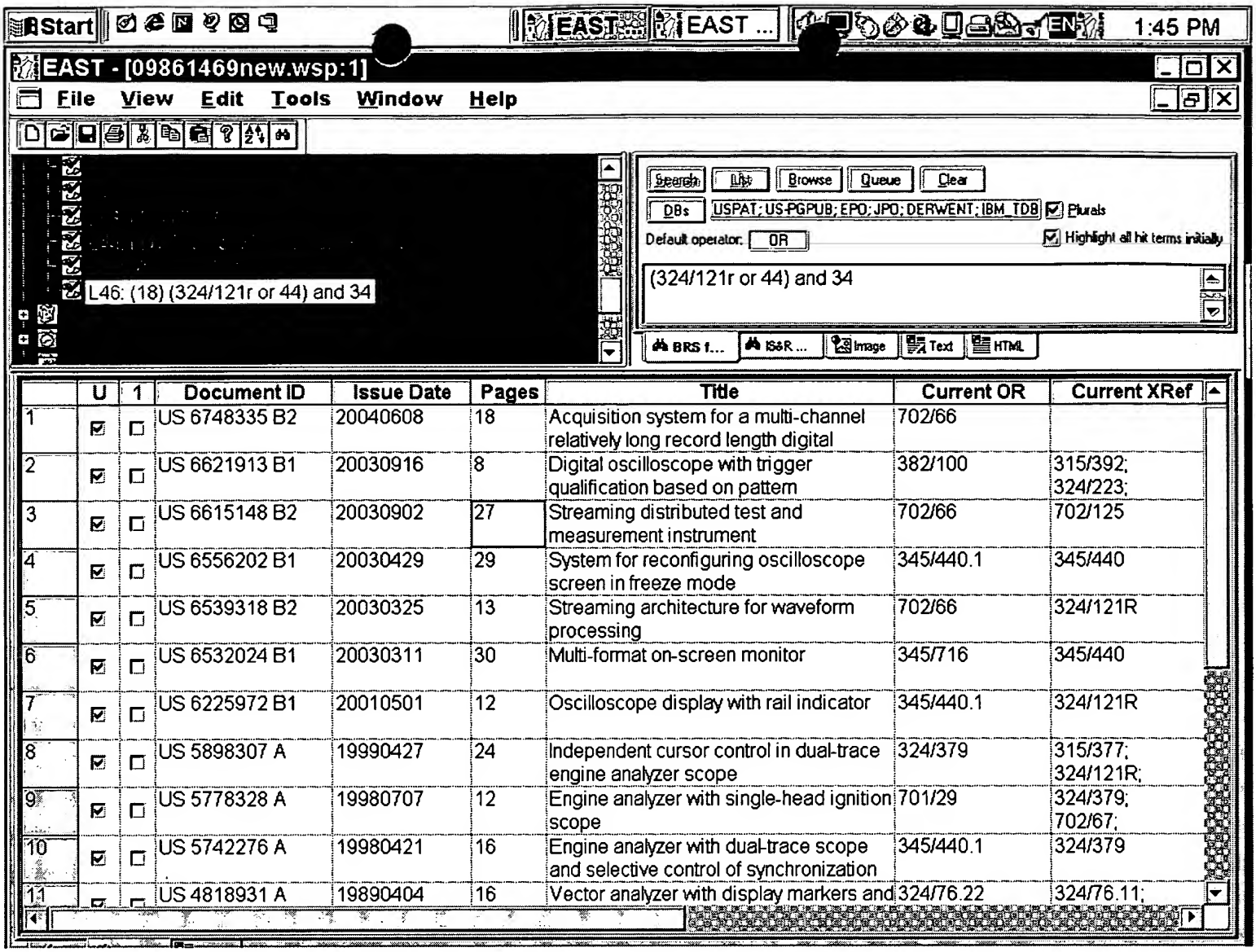
(51) Int. Cl.[7] G06K 9/36; H03 3/00; H04L 1/20; H04B 17/00

(52) U.S. Cl. 375/240; 348/441.1; 375/241; 375/243

(57) ABSTRACT

A digital signal transmission system using a digital modulation system comprising a digital signal transmitter having a first digital signal processing unit and a digital signal receiver, a digital signal from the transmitter, wherein the digital signal receiver comprising a second digital signal processing unit for processing the digital signal from the transmitter and comprising a digital demodulated signal and a modulation value signal, a signal converter coupled with the second digital signal processing unit and supplied the modulation value signal therefrom for generating a waveform indicating a transmission condition including a main wave in response to the modulation value signal, and a display coupled with the signal converter for displaying the waveform indicating a transmission condition in the digital transmission system.





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